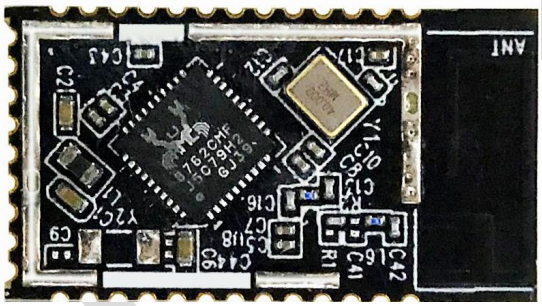
RB8762-35P

Bluetooth Module



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1. Device Overview

1.1 Features

- Ultra-low consumption with intelligent PMU
- Supports Bluetooth 5.0 core specification
- Supports 2Mbps LE
- LE advertising extensions
- LE long range
- Additional Adv channel
- High duty cycle non-connectable Adv
- Supports multiple level low energy states
- Supports LE L2CAP connection oriented channel support
- Supports GAP, ATT/GATT, SMP, L2CAP
- Supports LE low duty directed advertising
- Supports LE data length extension feature
- Supports OTA programming mechanism for firmware upgrade

1.2 Applications

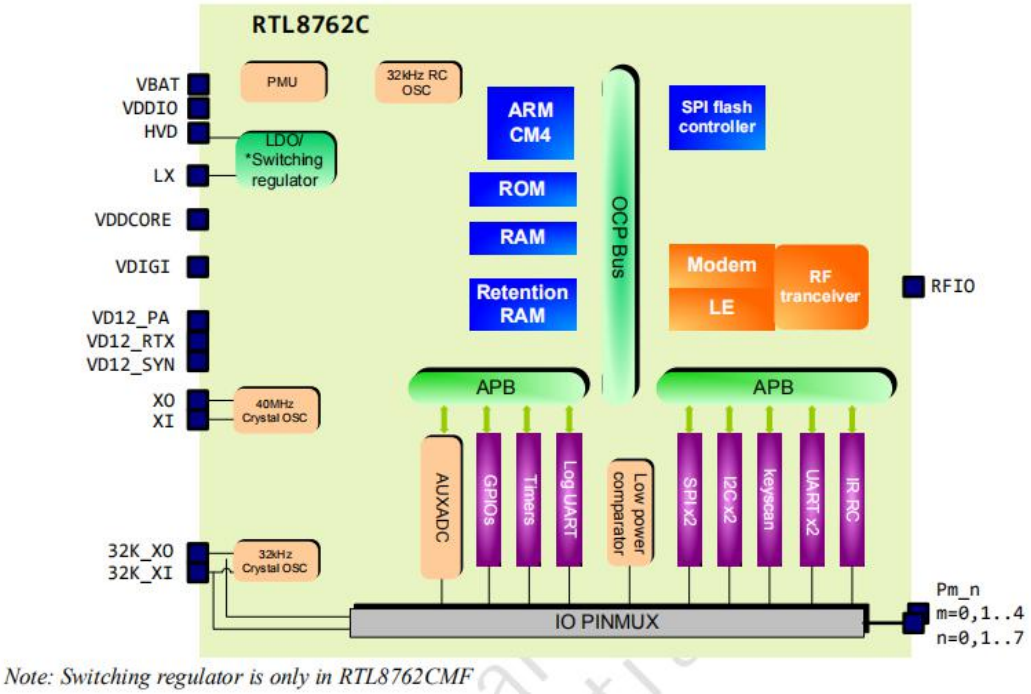
- Mesh LED
- Mice and wireless keyboards
- Game controllers & joysticks
- Voice remote controls
- Home automation
- Sensor network devices
- Amazon gadgets
- Intelligent Lighting

1.3 Descriptions

The RB8762-35P Bluetooth module is designed base on the Realtek RTL8762CMF that is an ultra-low power system on-chip solution for Bluetooth 5.0 low energy applications. It combines the excellent performance of a leading RF transceiver with a low-power ARM Cortex-M4F and rich powerful supporting features and peripherals. The embedded ARM Cortex-M4F 32-bit CPU features a 16-bit instruction set with 32-bit extensions (Thumb-2® technology) that delivers high-density code with a small memory footprint. By using a single-cycle 32-bit multiplier, a 3-stage pipeline, and a Nested Vector Interrupt Controller (NVIC), the ARMCortex-M4F makes program execution simple and highly efficient.

The RB8762-35P module consists of three major parts: PCB antenna, 40MHz crystal and RTL8762CMF BLE chip. All of the module materials can withstand an ultimate ambient temperature of 105℃ which makes the module very suitable for lamps or other occasions with high temperature requirements.

1.4 Functional Block Diagram



Note: Switching regulator is only in RTL8762CMF

Figure 1. Block Diagram of RTL8762CMF

2. Pin Configuration and Functions

2.1 Module Pin Diagram

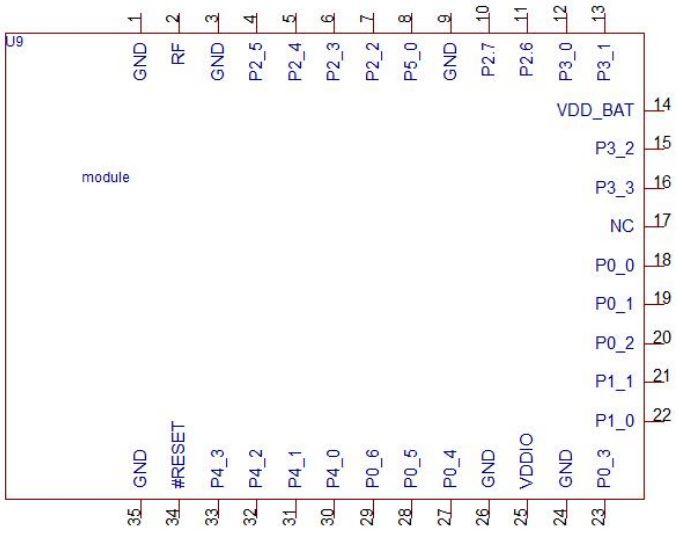


Figure 2. Pin Diagram of RB8762-35P

2.2 Pin Functions

Pin	Name	Hardware Default Pull setting(100K)Reset state	Description
1	GND	Ground	Ground
2	RF	RF	RF interface
3	GND	Ground	Ground
4	P2_5	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down AUXADC input 5
5	P2_4	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down AUXADC input 4
6	P2_3	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down AUXADC input 3
7	P2_2	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down AUXADC input 2
8	P5_0	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
9	GND	Ground	Ground
10	P2_7	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down AUXADC input 7
11	P2_6	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down AUXADC input 6
12	P3_0	Pull Up	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down HCI_UART_TX(default)
13	P3_1	Pull Up	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down HCI_UART_RX(default)

14	VDD_BAT	power	Supply 1.8V~3.3V
15	P3_2	Pull Up	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
16	P3_3	Pull Up	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
17	NC	NC	NC
18	P0_0	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
19	P0_1	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
20	P0_2	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
21	P1_1	Pull Up	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down SWDCLK(default)
22	P1_0	Pull Up	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down SWDIO(default)
23	P0_3	Pull Up	LOG_UART_TX Power on trap: Pull-up for normal operation Pull-down to bypass executing program code in flash
24	GND	Ground	Ground
25	VDDIO	Power	Supply 1.8V~3.3V power for digital IO PADs VDDIO should be less than or equal to VDD_BAT
26	GND	Ground	• GPIO: P12 • Keyboard scan output (column): KSO4 • A/D converter input 23
27	P0_4	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
28	P0_5	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
29	P0_6	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down

30	P4_0	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
31	P4_1	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
32	P4_2	Pull Down	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
33	P4_3	Pull Up	General purpose IO; refer to the Pin Multiplexer Table 8mA driving capability With wakeup function With inter strong/weak pull-up and pull-down
34	RESET		Hardware reset pin, low active
35	GND	Ground	Ground

Note: Pin Multiplexer

All GPIO pins are configurable via the built-in pin multiplexer(PINMUX), The table shows all GPIO pin configurations.All pins have an internal pull-up pull-down resistor for controlling GPIO_PU and GPIO_PD.

Pin Multiplexer Table

0	IDEL	25	qdec_phase_a_z	50	SPI0_CLK (master only)	75	KEY_COL_17	100	Reserved	125	Reserved
1	HCI_UART_TX	26	qdec_phase_b_z	51	SPI0_MO (master only)	76	KEY_COL_18	101	Reserved	126	Reserved
2	HCI_UART_RX	27	UART2_TX	52	SPI0_MI (master only)	77	KEY_COL_19	102	PDM (clk)	127	MCLK
3	HCI_UART_CTS	28	UART2_RX	53	SPI2W_DATA (master only)	78	KEY_ROW_0	103	PDM (data)		
4	HCI_UART_RTS	29	UART1_TX	54	SPI2W_CLK (master only)	79	KEY_ROW_1	104	UART2_CTS		
5	I2C0_CLK	30	UART1_RX	55	SPI2W_CS (master only)	80	KEY_ROW_2	105	UART2_RTS		
6	I2C0_DAT	31	UART1_CTS	56	SWD_CLK	81	KEY_ROW_3	106	Reserved		
7	I2C1_CLK	32	UART1_RTS	57	SWD_DIO	82	KEY_ROW_4	107	Reserved		
8	I2C1_DAT	33	IRDA_TX	58	KEY_COL_0	83	KEY_ROW_5	108	Reserved		
9	PWM2_P	34	IRDA_RX	59	KEY_COL_1	84	KEY_ROW_6	109	Reserved		
10	PWM2_N	35	UART0_TX	60	KEY_COL_2	85	KEY_ROW_7	110	Reserved		
11	PWM3_P	36	UART0_RX	61	KEY_COL_3	86	KEY_ROW_8	111	Reserved		
12	PWM3_N	37	UART0_CTS	62	KEY_COL_4	87	KEY_ROW_9	112	Reserved		
13	PWM0	38	UART0_RTS	63	KEY_COL_5	88	KEY_ROW_10	113	Reserved		
14	PWM1	39	SPI1_SS_N_0 (master only)	64	KEY_COL_6	89	KEY_ROW_11	114	Reserved		
15	PWM2	40	SPI1_SS_N_1 (master only)	65	KEY_COL_7	90	DWGPIO	115	Reserved		
16	PWM3	41	SPI1_SS_N_2 (master only)	66	KEY_COL_8	91	I2S_LRCLK	116	Reserved		
17	PWM4	42	SPI1_CLK (master only)	67	KEY_COL_9	92	I2S_BCLK	117	EN_EXPA		
18	PWM5	43	SPI1_MO (master only)	68	KEY_COL_10	93	I2S_ADCDAT	118	EN_EXLNA		
19	PWM6	44	SPI1_MI (master only)	69	KEY_COL_11	94	I2S_DACDAT	119	ANT_SW0		
20	PWM7	45	SPI0_SS_N_0 (slave)	70	KEY_COL_12	95	Reserved	120	ANT_SW1		
21	qdec_phase_a_x	46	SPI0_CLK (slave)	71	KEY_COL_13	96	DMIC1_CLK	121	ANT_SW2		
22	qdec_phase_b_x	47	SPI0_SO (slave)	72	KEY_COL_14	97	DMIC1_DAT	122	ANT_SW3		
23	qdec_phase_a_y	48	SPI0_SI (slave)	73	KEY_COL_15	98	Reserved	123	Reserved		
24	qdec_phase_b_y	49	SPI0_SS_N_0 (master only)	74	KEY_COL_16	99	Reserved	124	Reserved		

3. Specifications

3.1 Absolute Maximum Rating

1) Power supply voltage:

VDDIO: 1.8V~3.3V

VDD_BAT:1.8V~3.3V

Note: VDDIO should be less than or equal to VDD_BAT.

2) Operation temperature range: -30℃~+105℃

3) Storage temperature range: -40℃~+125℃

3.2 Power Consumption

Condition: VDD_BAT=3V, VDDIO=3V, Ambient Temperature: 25℃

1) Low Power Mode

Power Mode	Always on Registers	32k RCOSC/XTAL	Retention SRAM	CPU	Wakeup Method	Current Consumption(Typical)
Power down	ON	OFF	OFF	OFF	Wakeup by GPIO	450nA
Deep LPS	ON	ON	Retention	OFF	Wakeup by timer	2.5uA(with 160K SRAM in retention state)

2) Active Mode

Condition: VDD_BAT=3V, VDDIO=3V, Ambient Temperature: 25℃

Power Mode	Current Consumption(Typical)
Active RX mode	7.3mA
Active TX mode(TX power:0dBm)	7.9mA
Active TX mode(TX power:4dBm)	9.6mA
Active TX mode(TX power:7.5dBm)	11.3mA

3.3 RF Characteristics

1) Receiver RF Specifications

Parameter	Condition	Min.	Typ.	Max.
Frequency Range(MHz)		2402		2480
Sensitivity(dBm)	PER≤30.8%	-94		
Maximum Input Level(dBm)	PER≤30.8%		-1	
C/I	C/Ico-channel(dB)	21		
	C/I+1MHz(dB)	15		
	C/I-1MHz(dB)	15		
	C/I+2MHz(dB)	-17		

	C/I-2MHz(dB)	-15		
	C/I+3MHz(dB)	-27		
	C/IImage(dB)	-9		
	C/IImage+1MHz(dB)	-15		
	C/IImage-1MHz(dB)	-15		
Blocker Power(dBm)	30～2000MHz, Wanted signal level=-67dBm	-30		
	2003～2399MHz, Wanted signal level=-67dBm	-35		
	2484～2997MHz, Wanted signal level=-67dBm	-35		
	3000MHz～12.75GHz, Wanted signal level=-67dBm	-30		
Max PER Report Integrity	Wanted signal:-30dBm		50%	
Max Intermodulation level (dBm)	Wanted signal(f0):-64dBm Worst intermodulation level@2f1-f2=f0, |f1-f2|=nMHz, n=3,4,5…	-50		

Note1: Do not include spur channel;

Note2: Depend on PCB design and registers setting.

2) Transmitter RF Specifications

Parameter	Condition	Min.	Typ.	Max.
Maximum Output Power (dBm)	Conducted	-	-	8
Adjacent Channel Power Ratio (dBm)	+2MHz	-	-	-20
	-2MHz	-	-	-20
	≥+3MHz	-	-	-30
	≤-3MHz	-	-	-30
Modulation Characteristics	$\Delta f1_{avg}$(kHz)	-	250	-
	$\Delta f2_{max}$(kHz)	185	-	-
	$\Delta f2_{max}$	-	100	-
	$\Delta f2_{max}$PassRate(%)	-	0.88	-
Carrier Frequency Offset and Drift	Average Fn(kHz)	-	12.5	-
	Drift Rate(kHz/50us)	-	10	-
	Avg Rate(kHz/50us)	-	10	-
	Max Rate(kHz/50us)	-	10	-
Output power of second harmonic(dBm)	-	-	-50 （note）	-
Output power of third harmonic(dBm)	-	-	-50 （note）	-

Note：Tested by EVB with RF PI network.

4. Application, Implementation, and Layout

4.1 Application Diagram

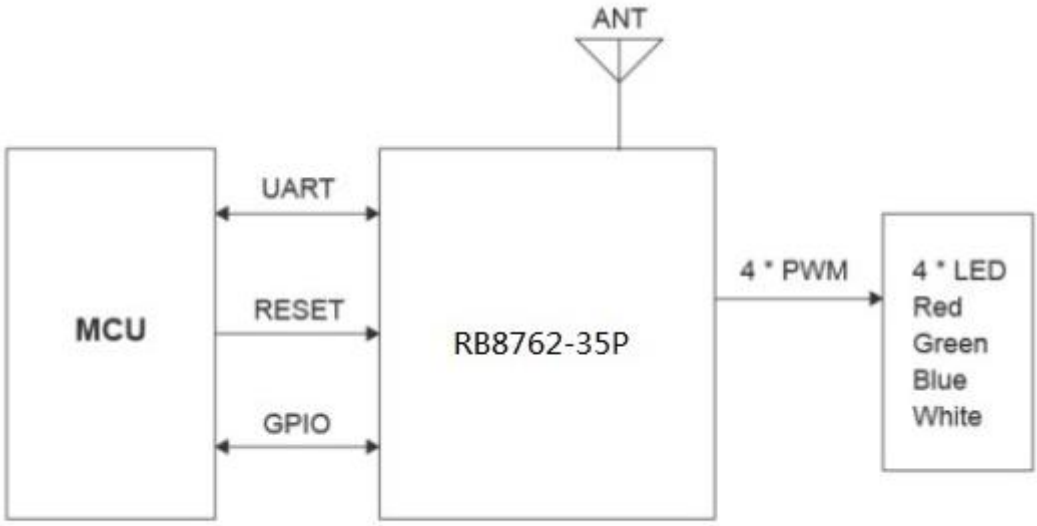


Figure 3. Remote Control Block Diagram of RB8762-35P

4.2 Typical Application Circuit

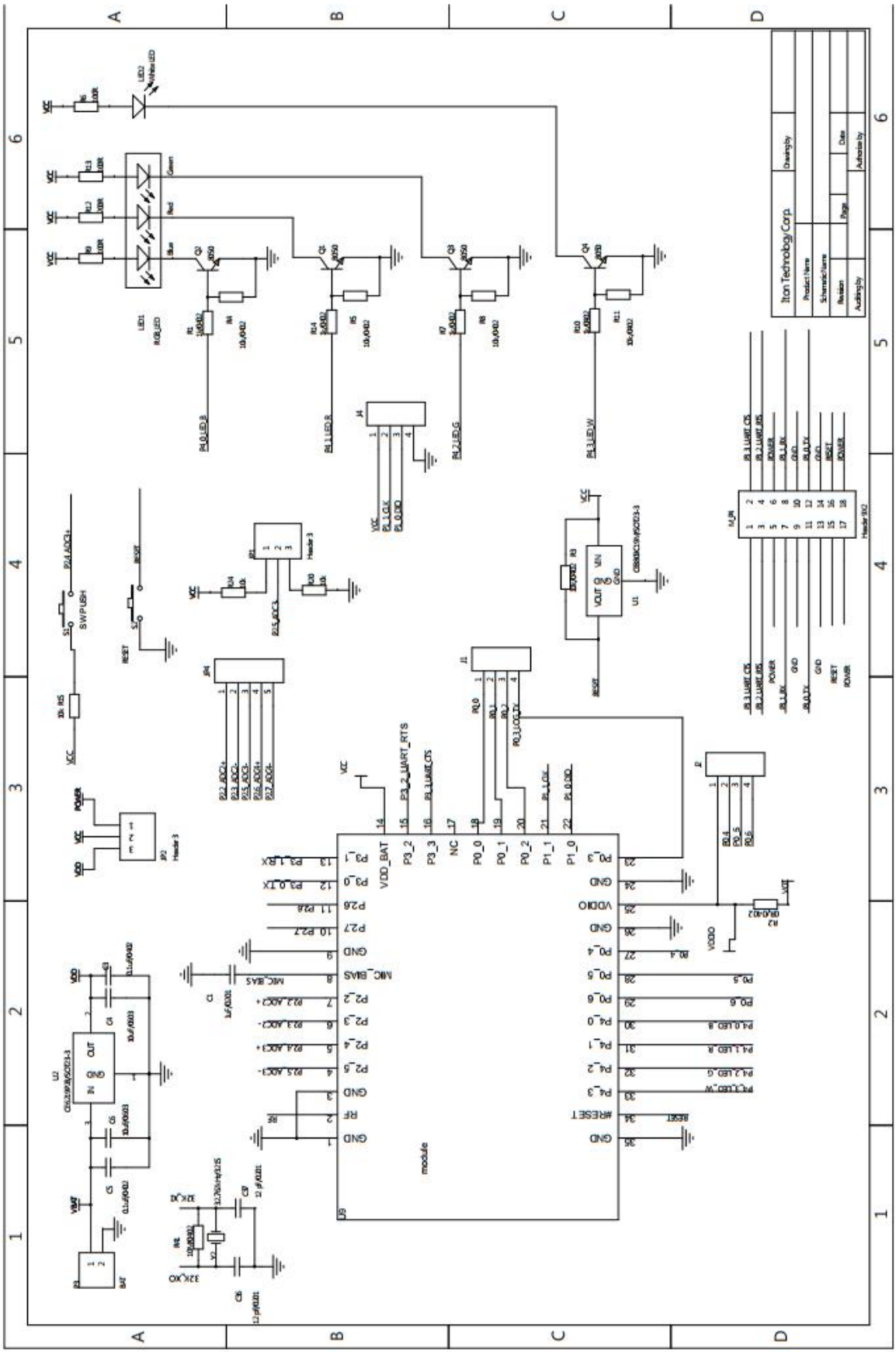


Figure 4. Mesh LED schematic of RB8762-35P

4.3 Layout Guideline

1. Keep RF traces with 50 Ohm impedance.
2. The antenna needs to have enough clearance area.
3. The filter capacitor should be as close as possible to the module.
4. Do not place strong interference lines under the module.
5. RF interface selection: Printed PCB antenna or RF PAD

A>: Printed PCB antenna: R1 NC/ R2 0R

B>: RF PAD: R1 0R/ R2 NC

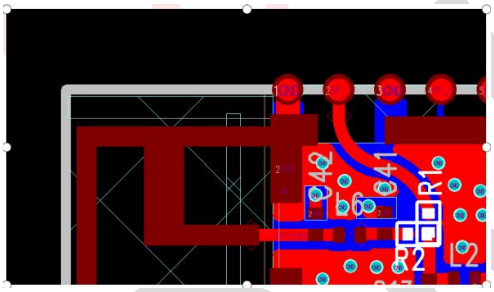


Figure 5. RF Interface Selection

5. Mechanical and Package

5.1 Mechanical Dimension

PCB thickness: 1.0mm. Module thickness: 2.0mm±0.25mm

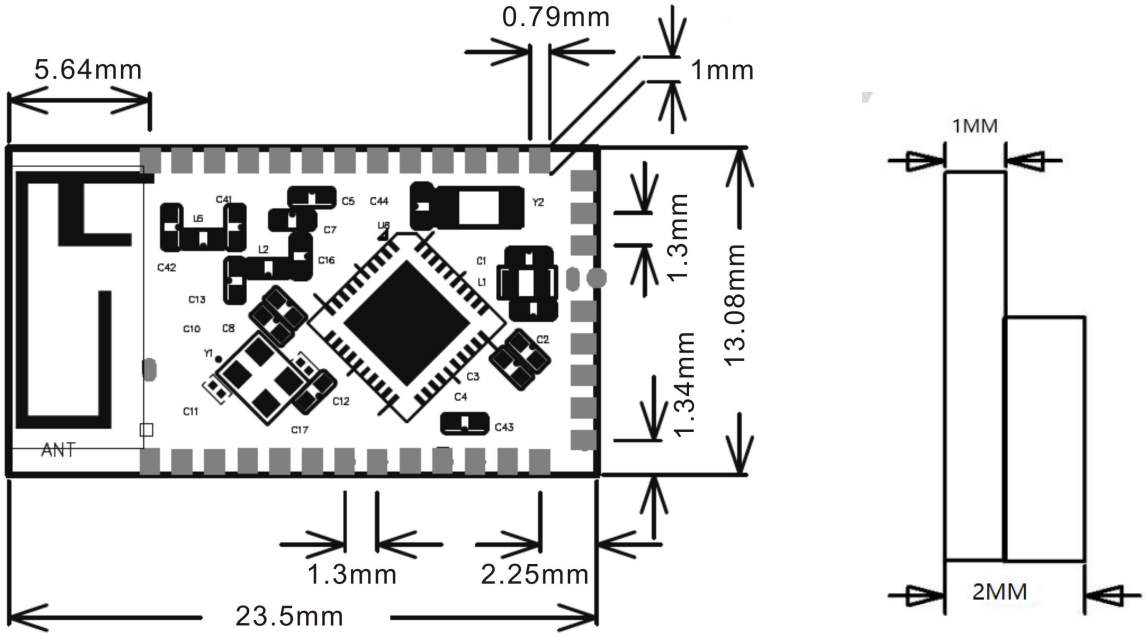


Figure 6. Mechanical Dimension of RB8762-35P

Note: Unit is mm. Size tolerance:±0.13mm.

5.2 Recommended PCB Footprint

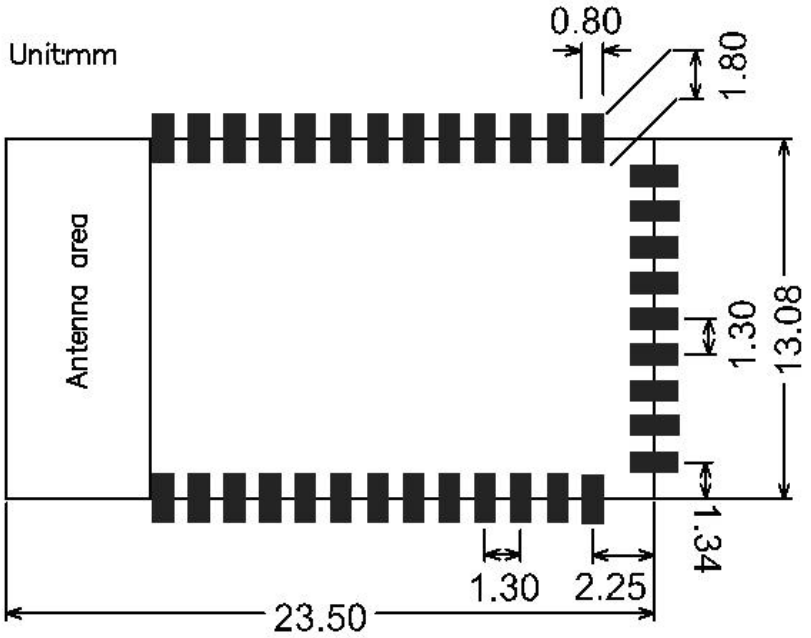


Figure 7. Recommended PCB Footprint of RB8762-35P

5.3 Package Information

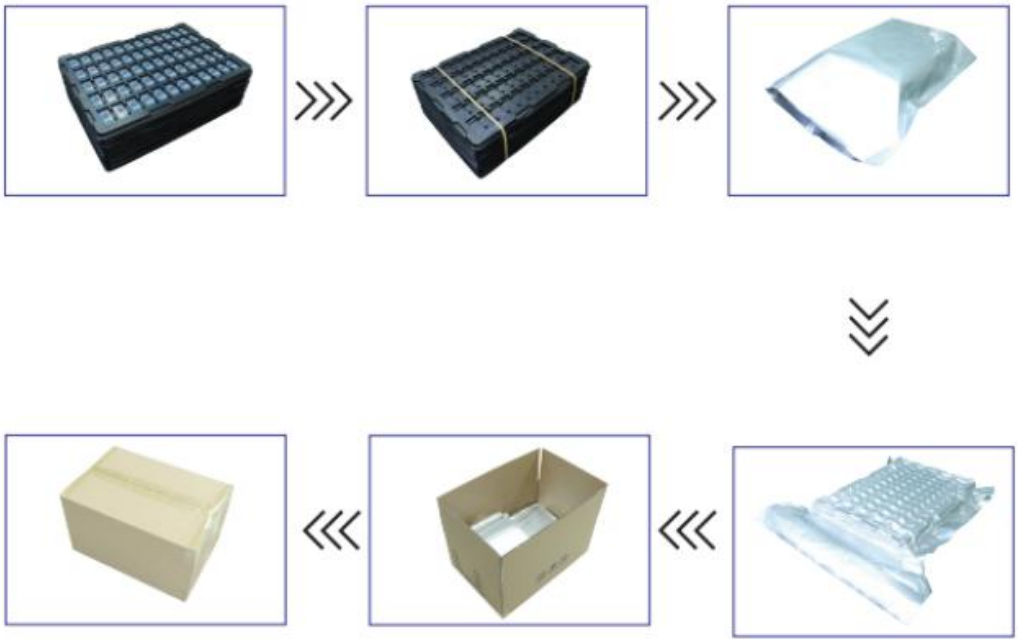


Figure 8. Brief Packaging Process of RB8762-35P Modules

6. Thermal Reflow

Referred to IPC/JEDEC standard.

Peak temperature: <250°C

Number of times: 6≤2

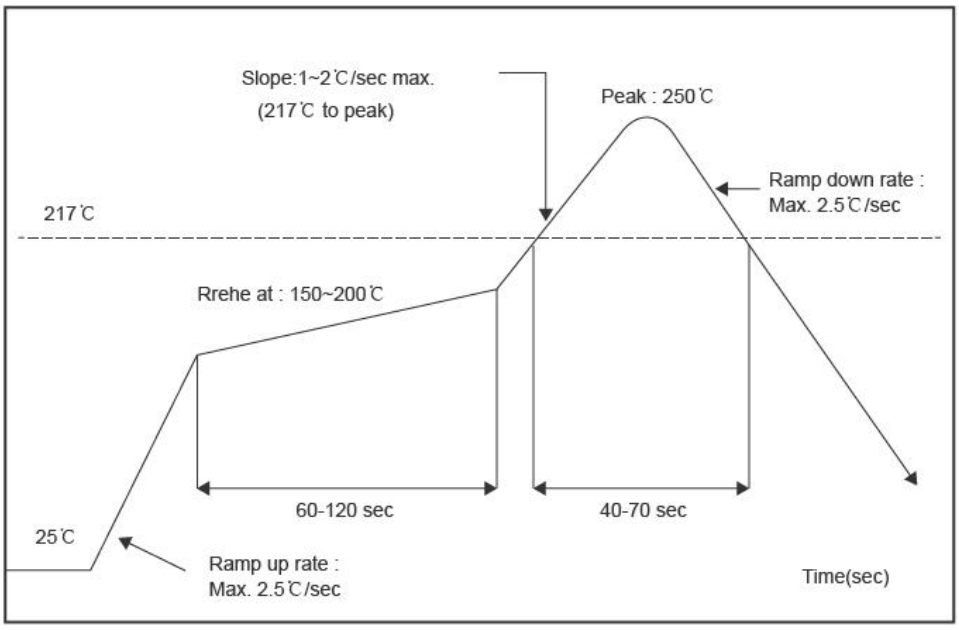


Figure 9. Recommended Reflow for Lead Free Solder

Note: The module is recommended not to go through reflow oven twice.

7. Ordering Information

Part NO.	Working Voltage	ANT	Shielding Cover	Remark
RB8762-35P	VDDIO:1.8V~3.3V VDD_BAT:1.8V~3.3V	PCB ANT	Not Included	
RB8762-35P1	VDDIO:1.8V~3.3V VDD_BAT:1.8V~3.3V	RF pin external antenna	Not Included	

8. Revision History

Version	Change Content	Reviser	Date
V1.0	Initial Version	Yongwu Zhong	2019.11.28
V2.0	Modified Mechanical Figure and Package	Yongwu Zhong	2020.04.24
V2.1	ADD Conducted TEST DATA	Yongwu Zhong	2020.05.08